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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/044,493	YU ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,20 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed May 25, 2004, with respect to the rejection(s)of claim(s) 1-10, 20, and 21 under 35 USC § 102, 112, and 103 have been fully considered. Newly amended claim 5 has overcome the rejection made under 35 USC § 112 and is hereby withdrawn. However the arguments concerning the rejection of claim(s) 1-10, 20, and 21 under 35 USC § 102 and 103 are not persuasive. The applicant states that Snyder uses an implanted channel layer below the source and the drain. However Snyder makes it clear that the channel is between the source and the drain by stating that the channel length in the substrate is 100 nm (claim 1). Furthermore Snyder states that the gate (906 or 907) has a length of 100 nm (claim 4), in order to correspond to the short channel length (column 10, lines 44-48). Therefore the rejection(s)of claim(s) 1-10 and 20 under 35 USC § 102 and 103 using the Snyder reference stands. In addition, a new ground(s) of rejection is made in view of the newly cited references discussed below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 5, 9, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Snyder (USPN 6,303,479 B1) in view of Ma et al. (USPN 6,060,755) and further in view of Liu et al. (USPN 6,590,271 B2).

4. In reference to claims 1, 2, and 5, Snyder (USPN 6,303,479 B1, hereinafter referred to as the "Snyder reference) discloses a similar device. Figure 9 of Snyder discloses a semiconductor device (904 or 905) with a source and a drain (904 or 905) consisting essentially of silicide. A semiconductor body is disposed between the source and the drain (904 or 905). There is a gate electrode (906 or 907) which is disposed over the body; it is understood that the gate electrode (906 or 907) defines a channel between the source and the drain (904 or 905). A gate dielectric separates the gate electrode (906 or 907) from the body. The examiner notes that the applicant has stated that titanium oxide, zirconium oxide, and barium strontium titanate each have a relative permittivity of 10 or more (p. 4 of specification, lines 18-29). Snyder does not disclose the use of a gate dielectric with a relative permittivity greater than 10. However the use of such high dielectric constant materials as the gate insulating film is well known in the art. Ma et al. (USPN 6,060,755, hereinafter referred to as the "Ma" reference) discloses that a gate insulating film made of high dielectric constant materials, such as titanium oxide and barium strontium titanate, allows smaller devices to be built (column 1, lines 13-30). Liu et al. (USPN 6,590,271 B2, hereinafter referred to as the "Liu" reference) discloses that smaller devices are desirable in the art (column 1, lines 15-22). In view of Ma and Liu, it would therefore be obvious to use either titanium oxide, zirconium oxide, or barium strontium titanate as the gate dielectric of Snyder.

5. With regard to claim 9, there is a liner which is disposed adjacent sidewalls defined by the gate electrode (906 or 907) and the gate dielectric.

6. In reference to claim 20, Snyder (USPN 6,303,479 B1) discloses a similar device. Figure 9 of Snyder discloses a semiconductor device (904 or 905) with a source and a drain (904 or 905) consisting essentially of silicide. A semiconductor body is disposed between the source and the drain (904 or 905). A source/body junction is defined by silicide material of the source and semiconductor material of the body. A drain/body junction is defined by silicide material of the drain and semiconductor material of the body. There is a gate electrode (906 or 907) which is disposed over the body; it is understood that the gate electrode (906 or 907) defines a channel between the source and the drain (904 or 905). A gate dielectric separates the gate electrode (906 or 907) from the body. The examiner notes that the applicant has stated that titanium oxide, zirconium oxide, and barium strontium titanate each have a relative permittivity of 10 or more (p. 4 of specification, lines 18-29). Snyder does not disclose the use of a gate dielectric with a relative permittivity greater than 10. However the use of such high dielectric constant materials as the gate insulating film is well known in the art. Ma (USPN 6,060,755) discloses that a gate insulating film made of high dielectric constant materials, such as titanium oxide and barium strontium titanate, allows smaller devices to be built (column 1, lines 13-30). Liu (USPN 6,590,271 B2) discloses that smaller devices are desirable in the art (column 1, lines 15-22). In view of Ma and Liu, it would therefore be obvious to use either titanium oxide, zirconium oxide, or barium strontium titanate as the gate dielectric of Snyder.

7. In reference to claim 21, Snyder (USPN 6,303,479 B1) discloses a similar device. Figure 9 of Snyder discloses a semiconductor device (904 or 905) with a source and a drain (904 or 905) consisting of silicide. A semiconductor body is disposed between the source and the drain (904 or 905). There is a gate electrode (906 or 907) which is disposed over the body; it is understood that the gate electrode (906 or 907) defines a channel between the source and the drain (904 or 905). A gate dielectric separates the gate electrode (906 or 907) from the body. The examiner notes that the applicant has stated that titanium oxide, zirconium oxide, and barium strontium titanate each have a relative permittivity of 10 or more (p. 4 of specification, lines 18-29). Snyder does not disclose the use of a gate dielectric with a relative permittivity greater than 10. However the use of such high dielectric constant materials as the gate insulating film is well known in the art. Ma (USPN 6,060,755) discloses that a gate insulating film made of high dielectric constant materials, such as titanium oxide and barium strontium titanate, allows smaller devices to be built (column 1, lines 13-30). Liu (USPN 6,590,271 B2) discloses that smaller devices are desirable in the art (column 1, lines 15-22). In view of Ma and Liu, it would therefore be obvious to use either titanium oxide, zirconium oxide, or barium strontium titanate as the gate dielectric of Snyder.

8. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Snyder (USPN 6,303,479 B1) in view of Ma et al. (USPN 6,060,755) and further in view of Liu et al. (USPN 6,590,271 B2) as applied to claim 1 above and further in view of Wilk et al. (USPN 6,291,282 B1).

9. With regard to claims 3 and 4, Snyder does not disclose the use of a metal gate. However the use of a metal gate is well known in the semiconductor art. Wilk et al. (USPN 6,291,282 B1, hereinafter referred to as the "Wilk" reference) discloses that metal gates (such as tungsten, aluminum, and platinum) have a low sheet resistivity (column 1, lines 49-67 and column 2, lines 1-9). Wilk discloses that gates with low sheet resistivity are desirable in the art (column 1, lines 29-42). In view of Wilk, it would therefore be obvious to use a metal (such as tungsten, aluminum, and platinum) for the gate electrode.

10. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Snyder (USPN 6,303,479 B1) in view of Ma et al. (USPN 6,060,755) and further in view of Liu et al. (USPN 6,590,271 B2) as applied to claim 1 above and further in view of Raajimakers et al. (United States Patent Application Publication No. US 2001/0031562 A1).

11. In reference to claims 6 and 7, Snyder does not disclose the use of an oxide buffer layer. However it is well known in the art to provide an oxide buffer layer between a substrate and a high dielectric constant insulating film. Raajimakers discloses that a thin silicon oxide layer improves the interface between silicon and a high dielectric constant film (p.1, paragraph 7 and p.3, paragraph 33). It would therefore be obvious to use an oxide buffer layer in the device of Snyder constructed in view of Ma and Liu so as to attain this benefit. Snyder, Ma, Liu, and Raajimakers teach all of the claimed invention except for the exact thickness of the oxide layer. Although Snyder, Ma, Liu, and Raajimakers do not teach the exact oxide thickness as that claimed by Applicant:

> The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note In re Leshin, 125 USPQ 416.

Therefore claim 7 is not patentably distinguishable over the Snyder, Ma, Liu, and Raajimakers references.

12. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Snyder (USPN 6,303,479 B1) in view of Ma et al. (USPN 6,060,755) and further in view of Liu et al. (USPN 6,590,271 B2) as applied to claim 1 above and further in view of Poon et al. ("Thermal stability of cobalt and nickel silicides in amorphous and crystalline silicon," Proceedings of Electron Devices Meeting, 1997, p. 65-68).

13. In reference to claim 8, Snyder uses rare earth metal silicides for the source and drain but does not explicitly disclose the use of nickel silicide for the source and drain. However the use of nickel silicides is well known in the art. Poon et al. ("Thermal stability of cobalt and nickel silicides in amorphous and crystalline silicon," Proceedings of Electron Devices Meeting, 1997, p. 65-68, hereinafter referred to as the "Poon" reference) discloses that nickel silicide has the advantages of good thermal stability, a low formation temperature and a single step anneal (abstract). In view of Poon, it would therefore be obvious to use nickel silicide in the device of Snyder.

14. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Snyder (USPN 6,303,479 B1) in view of Ma et al. (USPN 6,060,755) and further in view of Liu et al. (USPN 6,590,271 B2) as applied to claim 1 above and further in view of Venkatesan et al. (USPN 5,736,435).

15. In reference to claim 10, Snyder does not disclose the use of an SOI substrate (a semiconductor film disposed on an insulating layer, the layer being disposed on a semiconductor substrate). However the use of an SOI substrate is well known in the art. Venkatesan et al. (USPN 5,736,435, hereinafter referred to as the "Venkatesan" reference) discloses that SOI provides the advantages of reduced junction capacitance, large drive currents, high transconductance values, and immunity to short channel effects (column 1, lines 35-55). It would therefore be obvious to construct the device of Snyder on an SOI substrate so as to attain these benefits.

16. Claims 1-3, 5, 8, 9, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (USPN 6,555,424 B2) in view of Ma et al. (USPN 6,060,755) and further in view of Liu et al. (USPN 6,590,271 B2).

17. In reference to claims 1-3 and 5, Lin et al. (USPN 6,555,424 B2, hereinafter referred to as the "Lin" reference) discloses a similar device. Figures 8a- 8g of Lin illustrate a MOSFET with a source (85a) and a drain (85b) consisting essentially of silicide. A semiconductor body (ch6) is disposed between the source (85a) and the drain (85b). A metal gate electrode (83) is disposed over the body (ch6) and defines a channel interposed between the source and the drain. A gate dielectric (82) separates the gate electrode (83) and the body (ch6). Lin does not disclose the use of a gate dielectric with a relative permittivity greater than 10. However the use of such high dielectric constant materials as the gate insulating film is well known in the art. Ma (USPN 6,060,755) discloses that a gate insulating film made of high dielectric constant materials, such as titanium oxide and barium strontium titanate, allows smaller devices

to be built (column 1, lines 13-30). Liu (USPN 6,590,271 B2) discloses that smaller devices are desirable in the art (column 1, lines 15-22). In view of Ma and Liu, it would therefore be obvious to use either titanium oxide, zirconium oxide, or barium strontium titanate as the gate dielectric of Lin.

18. With regard to claim 8, the silicide of the source and the drain is formed by reacting nickel with a layer of semiconductor material that forms the body of the semiconductor device (column 9, lines 43-48).

19. In reference to claim 9, there is a liner (84) which is disposed adjacent sidewalls defined by the gate electrode (83) and the gate dielectric (82).

20. In reference to claim 20, Lin (USPN 6,555,424 B2) discloses a similar device. Figures 8a-8g of Lin disclose a semiconductor device with a source (85a) and a drain (85b) consisting essentially of silicide. A semiconductor body is disposed between the source (85a) and the drain (85b). A source/body junction is defined by silicide material of the source and semiconductor material of the body. A drain/body junction is defined by silicide material of the drain and semiconductor material of the body. There is a gate electrode (83) which is disposed over the body. The gate electrode (83) defines a channel (column 9, lines 51-55) between the source (85a) and the drain (85b). A gate dielectric (82) separates the gate electrode (83) from the body. The examiner notes that the applicant has stated that titanium oxide, zirconium oxide, and barium strontium titanate each have a relative permittivity of 10 or more (p. 4 of specification, lines 18-29). Lin does not disclose the use of a gate dielectric with a relative permittivity greater than 10. However the use of such high dielectric constant materials as the gate

insulating film is well known in the art. Ma (USPN 6,060,755) discloses that a gate insulating film made of high dielectric constant materials, such as titanium oxide and barium strontium titanate, allows smaller devices to be built (column 1, lines 13-30). Liu (USPN 6,590,271 B2) discloses that smaller devices are desirable in the art (column 1, lines 15-22). In view of Ma and Liu, it would therefore be obvious to use either titanium oxide, zirconium oxide, or barium strontium titanate as the gate dielectric of Lin.

21. In reference to claim 21, Lin (USPN 6,555,424 B2) discloses a similar device. Figures 8a-8g of Lin disclose a semiconductor device with a source (85a) and a drain (85b) consisting of silicide. A semiconductor body is disposed between the source (85a) and the drain (85b). There is a gate electrode (83) which is disposed over the body. The gate electrode (83) defines a channel (column 9, lines 51-55) between the source (85a) and the drain (85b). A gate dielectric separates the gate electrode (906 or 907) from the body. The examiner notes that the applicant has stated that titanium oxide, zirconium oxide, and barium strontium titanate each have a relative permittivity of 10 or more (p. 4 of specification, lines 18-29). Lin does not disclose the use of a gate dielectric with a relative permittivity greater than 10. However the use of such high dielectric constant materials as the gate insulating film is well known in the art. Ma (USPN 6,060,755) discloses that a gate insulating film made of high dielectric constant materials, such as titanium oxide and barium strontium titanate, allows smaller devices to be built (column 1, lines 13-30). Liu (USPN 6,590,271 B2) discloses that smaller devices are desirable in the art (column 1, lines 15-22). In view of Ma and Liu, it would

therefore be obvious to use either titanium oxide, zirconium oxide, or barium strontium titanate as the gate dielectric of Lin.

22. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (USPN 6,555,424 B2) in view of Ma et al. (USPN 6,060,755) and further in view of Liu et al. (USPN 6,590,271 B2) as applied to claim 1 above and further in view of Wilk et al. (USPN 6,291,282 B1).

23. With regard to claim 4, Lin does not disclose the exact material for the metal gate. However the use of a metal gate is well known in the semiconductor art. Wilk (USPN 6,291,282 B1) discloses that metal gates (such as tungsten, aluminum, and platinum) have a low sheet resistivity (column 1, lines 49-67 and column 2, lines 1-9). Wilk discloses that gates with low sheet resistivity are desirable in the art (column 1, lines 29-42). In view of Wilk, it would therefore be obvious to use a metal (such as tungsten, aluminum, and platinum) for the gate electrode.

24. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (USPN 6,555,424 B2) in view of Ma et al. (USPN 6,060,755) and further in view of Liu et al. (USPN 6,590,271 B2) as applied to claim 1 above and further in view of Raajimakers et al. (United States Patent Application Publication No. US 2001/0031562 A1).

25. In reference to claims 6 and 7, Lin does not disclose the use of an oxide buffer layer. However it is well known in the art to provide an oxide buffer layer between a substrate and a high dielectric constant insulating film. Raajimakers discloses that a thin silicon oxide layer improves the interface between silicon and a high dielectric

constant film (p.1, paragraph 7 and p.3, paragraph 33). It would therefore be obvious to use an oxide buffer layer in the device of Lin constructed in view of Ma and Liu so as to attain this benefit. Lin, Ma, Liu, and Raajimakers teach all of the claimed invention except for the exact thickness of the oxide layer. Although Lin, Ma, Liu, and Raajimakers do not teach the exact oxide thickness as that claimed by Applicant:

> The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note In re Leshin, 125 USPQ 416.

Therefore claim 7 is not patentably distinguishable over the Lin, Ma, Liu, and Raajimakers references.

26. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (USPN 6,555,424 B2) in view of Ma et al. (USPN 6,060,755) and further in view of Liu et al. (USPN 6,590,271 B2) as applied to claim 1 above and further in view of Rissman et al. (USPN 5,661,043).

27. In reference to claim 10, Lin does not disclose the use of SOI (semiconductor on insulator formed on a silicon substrate). However the use of such a substrate is well known in the art. Rissman et al. (USPN 5,661,043, hereinafter referred to as the "Rissman" reference) discloses an SOI substrate in figure 5 and discloses that SOI provides the advantage of reduced junction capacitance which leads to increased circuit speed (column 1, lines 27-33). It would therefore be obvious to construct the device of Lin on an SOI substrate so as to attain these benefits.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

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